AMENDMENTS TO THE CLAIMS:

Please cancel claims 5, 7-9 and 34 without prejudice or disclaimer.

1. (Currently amended) A method of analyzing voltage drops on at least one power grid ~~power distribution~~ in an integrated circuit chip, comprising:

dividing a clock cycle of said integrated circuit chip into a plurality of time periods;

~~dividing said integrated circuit chip into a plurality of cells;~~

performing a static timing analysis ~~for said plurality of cells~~ to obtain current waveform data for said plurality of time periods for a plurality of cells of said integrated circuit chip ~~each cell and each time period~~; and

performing at least one simulation of said at least one power grid using extracted power grid information, placement information for said plurality of cells, and said current waveform data to calculate at least one voltage at a plurality of locations within said power grid ~~a power distribution analysis using said current waveform data~~.

2. (Currently amended) The method according to claim 1, wherein said performing said static timing analysis comprises using pre-characterized cell library information ~~further comprising:~~

~~generating a pre-characterized cell library comprising cell characterization data; and using said cell characterization data to perform said static timing analysis~~.

3. (Currently amended) The method according to claim 1 ~~2~~, further comprising:

computing at least one current density on at least one element of said power grid ~~wherein said cell characterization data comprises charge data, timing data, voltage data, temperature data, load data, input slew rate data, direct current data and process corner data~~.

4. (Currently amended) The method according to claim 3 ~~2~~, further comprising:

modifying said integrated circuit chip based on said at least one current density

~~physically designing said integrated circuit chip using said pre-characterized cell library~~.

5. (Canceled)

6. (Currently amended) The method according to claim 1 ~~4~~, further comprising:

modifying said integrated circuit chip based on said at least one voltage ~~wherein said current waveform data generated by an execution of said method is used to physically design said integrated circuit chip in a next execution of said method~~.

7-9. (Canceled)

10. (Currently amended) The method according to claim 1, wherein each of said time periods is greater than or equal to at least one of rise and fall times of a predetermined fraction ~~a rise or fall time that captures 95%~~ of signals on said integrated circuit chip.

11. (Currently amended) The method according to claim 1, wherein said at least one voltage comprises a voltage during each of said plurality of time periods ~~static timing analysis comprises:~~

~~assigning a charge used by a circuit to at least one time period; and~~

~~calculating node voltages for each time period~~.

12. (Currently amended) The method according to claim 3 ~~11~~, further comprising: ~~wherein said static timing analysis further comprises:~~

checking said ~~calculated node~~ voltages against allowable limits;

~~calculating current densities using said calculated node voltages;~~ and

checking said at least one current density against at least one of ~~calculated node voltages against~~ electromigration limits and local heating rules.

13. (Currently amended) The method according to claim 1 ~~11~~, further comprising:

performing another static timing analysis using said at least one voltage determined in said performing said at least one simulation of said at least one power grid

~~wherein node voltages calculated during a run of said static timing analysis are back annotated in a next run of said static timing analysis to re-calculate node voltages.~~

14. (Currently amended) The method according to claim 1, further comprising:

~~wherein said performing a power distribution analysis comprises~~ generating a graphical map of said at least one voltage and said plurality of locations ~~a power distribution~~.

15. (Previously presented) A system for analyzing power distribution in an integrated circuit chip comprising:

a chip design device for using pre-characterized cell data to logically and physically design said integrated circuit chip;

a power grid extracting device, for inputting physical design data from said chip design device and generating extracted signal net information; and

a static timing analysis tool, for dividing a clock cycle of said integrated circuit chip into a plurality of time periods, and inputting said extracted signal net information and said physical design data and generating current waveform data for said time periods.

16. (Original) The system according to claim 15, further comprising:

a power distribution analysis tool, for inputting said current waveform data and generating power distribution data.

17. (Currently amended) The method ~~of~~ according to claim 6, wherein said method is performed by using a digital data processing apparatus.

18. (Currently amended) A programmable storage medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to perform a method

of analyzing voltage drops on at least one power grid ~~power distribution~~ in an integrated circuit chip, said method comprising:

dividing a clock cycle of said integrated circuit chip into a plurality of time periods;

~~dividing said integrated circuit chip into a plurality of cells;~~

performing a static timing analysis ~~for said plurality of cells~~ to obtain current waveform data for said plurality of time periods for a plurality of cells of said integrated circuit chip ~~each cell and each time period~~; and

performing at least one simulation of said at least one power grid using extracted power grid information, placement information for said plurality of cells, and said current waveform data to calculate at least one voltage at a plurality of locations within said power grid ~~a power distribution analysis using said current waveform data~~.

19. (Previously presented) The system according to claim 15, wherein said pre-characterized cell data is included within a pre-characterized cell library.

20. (Original) The system according to claim 15, wherein said pre-characterized cell data comprises charge data, timing data, voltage data, temperature data, load data, input slew rate data, direct current data and process corner data.

21. (Original) The system according to claim 15, wherein said power grid extracting device extracts parasitic resistors, capacitors and inductors from a physical design of said integrated circuit chip to generate extracted signal net information.

22. (Original) The system according to claim 15, wherein said current waveform data generated during an operation of said system is input to said chip design device during a next operation of said system to refine a physical design of said integrated circuit chip.

23. (Original) The system according to claim 15, wherein said static timing analysis tool

determines when a current is required on said integrated circuit chip, an amount of current required on said integrated circuit chip, and where current is required on said integrated circuit chip.

24. (Original) The system according to claim 15, wherein every circuit on said integrated circuit chip switches within a given clock cycle.

25. (Original) The system according to claim 15, wherein said static timing analysis tool disregards circuits which cannot switch during a same time period.

26. (Previously presented) The system according to claim 15, wherein each of said time periods is greater than or equal to a rise or fall time that captures 95% of signals on said integrated circuit chip.

27. (Original) The system according to claim 15, wherein said static timing analysis tool assigns a charge used by a circuit to at least one time period, and calculates node voltages for each time period.

28. (Original) The system according to claim 27, wherein said static timing analysis tool checks calculated node voltages against allowable limits, electromigration rules and local heating rules, and calculates current densities using said calculated node voltages.

29. (Original) The system according to claim 28, wherein node voltages calculated during a static timing analysis are back annotated into said static timing analysis tool during a next static timing analysis to re-calculate node voltages.

30. (Original) The system according to claim 16, wherein said power distribution analysis tool generates a graphical map of a power distribution on said integrated circuit chip.

31. (Currently amended) The programmable storage medium according to claim 18, wherein said performing said static timing analysis comprises using pre-characterized cell library information ~~method further comprises:~~

~~generating a pre-characterized cell library comprising cell characterization data; and~~

~~using said cell characterization data to perform said static timing analysis.~~

32. (Currently amended) The programmable storage medium according to claim 31, wherein said method further comprises:

computing at least one current density on at least one element of said power grid ~~wherein said cell characterization data comprises charge data, timing data, voltage data, temperature data, load data, input slew rate data, direct current data and process corner data~~.

33. (Currently amended) The programmable storage medium according to claim 31, wherein said method further comprises:

modifying said integrated circuit chip based on said at least one current density

~~physically designing said integrated circuit chip using said pre-characterized cell library~~.

34. (Canceled)

35. (Currently amended) The programmable storage medium according to claim 18 ~~33~~, wherein said method further comprises:

modifying said integrated circuit chip based on said at least one voltage ~~wherein said current waveform data generated by an execution of said method is used to physically design said integrated circuit chip in a next execution of said method~~.

36. (Original) The programmable storage medium according to claim 18, wherein said static timing analysis comprises:

disregarding circuits which cannot switch during a same time period.

37. (Currently amended) The programmable storage medium according to claim 18, wherein said at least one voltage comprises a voltage during each or said plurality of time periods ~~static timing analysis comprises:~~

~~assigning a charge used by a circuit to at least one time period; and~~

~~calculating node voltages for each time period.~~

38. (Currently amended) The programmable storage medium according to claim 32 ~~18~~, wherein said method ~~static timing analysis~~ further comprises:

checking said ~~calculated node~~ voltages against allowable limits;

~~calculating current densities using said calculated node voltages;~~ and

checking said at least one current density against at least one of ~~calculated node voltages against~~ electromigration limits and local heating rules.

39. (Currently amended) The programmable storage medium according to claim 38, performing another static timing analysis using said at least one voltage determined in said performing said at least one simulation of said at least one power grid

~~wherein node voltages calculated during a run of said static timing analysis are back annotated in a next run of said static timing analysis to re-calculate node voltages.~~

40. (Currently amended) The programmable storage medium according to claim 18, wherein said method further comprises:

~~performing a power distribution analysis comprises~~ generating a graphical map of said at least one voltage and said plurality of locations ~~a power distribution on said integrated circuit chip.~~